CHIPIX65

CALL Project Proposal 2013 - Commissione Scientifica Nazionale 5
Istituto Nazionale Fisica Nucleare

SHORT ABSTRACT

The goal of this three years project is the development of an innovative CHIP for a PIXel detector, using a CMOS 65nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. New circuits will be built and characterized, a digital architecture will be developed and eventually a final assembly of a first prototype will be made.

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1 FINANCE AND PROJECT ORGANIZATION

1.1 Project Name:

CHIPIX65

1.2 Research Area

Electronics

1.3 Scientific Project Leader

DEMARIA	NATALE
(Name)	(First Name)
Primo Ricercatore	INFN Torino
07/12/1966	
(Date of birth)	
011-6707335	demaria@to.infn.it
(telephone)	(e-mail)

1.4 List of Participant Research Units and their composition

CHIPIX65 is composed of seven research units and 36 members, of which 20 are IC designers. The number of full time equivalent is 10.2. In the following two tables are shown: in Table 1 the name of the units and the appointed local representatives; in Table 2 the composition of the entire project, with the percentage dedicated by each member to CHIPIX65 and to synergic projects, indicated as the LHC experiments CMS and ATLAS and the European Project AIDA for the WP on micro-electronics.

Unit		**Unit Responsible**	**FTE Unit**	**No. of members**	**No. of designer**	**Involvements in CHIPIX65**
1	Bari	LODDO Flavio	1.65	5	3	WP2, WP3
2	Milano	LIBERALI Valentino	1.0	3	3	WP2,WP3,WP4
3	Padova	BISELLO Dario	1.6	5	1	WP1,WP3
4	Pavia	TRAVERSI Gianluca	1.5	7	4	WP1,WP3,WP4
5	Perugia	PLACIDI Pisana	1.4	5	3	WP1,WP2
6	Pisa	PALLA Fabrizio	1.5	6	3	WP2,WP4
7	Torino	DEMARIA Natale	1.55	4	3	WP2,WP3,WP4
		TOTAL	10.2	36	20	

Table 1: List of Participant Research Units

	Unit	Name	Title	% in CHIPIX65	% in AIDA	% in CMS/ ATLAS
1	Bari	Ciciriello Fabio	Borse neolaureati ind. tecn	50%	-	-
2	Bari	Corsi Francesco	Prof. Ordinario	30%	-	-
3	Bari	De Robertis Giuseppe	Primo Tecnologo	20%	-	20% (C)
4	Bari	Loddo Flavio	Primo Tecnologo	25%	-	25% (C)
5	Bari	Tamma Camillo	Borse neolaureati ind. tecn	40%	-	40% (C)
6	Milano	Liberali Valentino	Prof. Associato	40%	-	60% (A)
7	Milano	Shojaii Seyedruhollah	Dottorando in via di associazione	30%	-	70% (A)
8	Milano	Stabile Alberto	Assegno di ricerca	30%	-	40% (A)
9	Padova	Bagatin Marta	Tecnologo Assegnista	30%	-	20% (C)
10	Padova	Bisello Dario	Prof. Ordinario	30%	-	70% (C)
11	Padova	Ding Lili	Borsista Post. doct.	30%	-	20% (C)
12	Padova	Giubilato Piero	Ricercatore Associato	30%	-	-
13	Padova	Paccagnella Alessandro	Prof. Ordinario	40%	-	30% (C)
14	Pavia	De Canio Francesco	Assegnista di ricerca	20%	-	30% (C)
15	Pavia	Fabris Lorenzo	Dottorando	20%	-	30% (C)
16	Pavia	Gaioni Luigi	Assegno di Ricerca	20%	-	80% (C)
17	Pavia	Manghisoni Massimo	Ricercatore Associato	20%	-	50% (C)
18	Pavia	Re Valerio	Prof. Ordinario	10%	20%	60% (C)
19	Pavia	Traversi Gianluca	Ricercatore Associato	20%	-	50% (C)
20	Pavia	Vacchi Carla	Ricercatore Associato	40%	-	20% (C)
21	Perugia	Bilei Gian Mario	Primo Ricercatore	20%	-	80% (C)
22	Perugia	Conti Elia	Dottorando	50%	-	20% (C)
23	Perugia	Menichelli Mauro	Ricercatore	20%	10%	70% (C)
24	Perugia	Passeri Daniele	Ricercatore Associato	20%	-	20% (C)
25	Perugia	Placidi Pisana	Ricercatore Associato	30%	-	20% (C)
26	Pisa	Palla Fabrizio	Primo Ricercatore	20%	-	75% (C)
27	Pisa	Magazzu Guido	Primo Tecnologo	30%	-	-
28	Pisa	Morsani Fabio	Primo Tecnologo	25%	5%	-
29	Pisa	Beccherle Roberto	Tecnologo	30%	-	70% (A)
30	Pisa	Minuti Massimo	Collaboratore Tecnico E.R	30%	-	-
31	Pisa	Grippo Maria Teresa	Borsa Ente Pubblico	15%	-	85% (C)
32	Torino	Demaria Natale	Primo Ricercatore	40%	-	60% (C)
33	Torino	Civera Pierluigi	Professore Associato	40%	-	-
34	Torino	Pacher Luca	Dottorando	40%	-	60% (C)
35	Torino	Rivetti Angelo	Primo Tecnologo	20%	-	-
36	Torino	Da Rocha Rolo Manuel	Dottorando	20%	-	-
			Total =	10.20	0.35	12.75

Table 2: Composition of Participant Units. In the last column (C) and (A) means participation to CMS and ATLAS respectively

1.5 Scientific Curricula of Project Leader and Work Package leaders

DEMARIA Natale: degree in physics with Laude on 1989 and PhD in Physics on 1994 at University of Torino; Research Officer at University of Oxford on 1994-97; Fellowship at CERN on 1998-99; INFN Researcher on 1998 and senior scientist on 2006 at Torino.

- 1994-1999 He worked the upgrade micro-vertex silicon detector for DELPHI experiment at Oxford, with responsibility in the construction of modules in UK and final assembly and testing at CERN. He has been responsible of the off-line reconstruction software of the pixel detector of the Very Forward Tracker of Delphi, for the micro-vertex upgrade of 1996.
- 1997-2000 R&D of the micro-strip detectors for the CMS-Tracker, in particular to the HV stability, the width over pitch optimisation and characterization for radiation damage. He studied the procedures for later sensor and module production testing.
- 2001-2007 He setup a CMS Tracker production centre in Torino, where 500 modules have been produced and tested, all the six Tracker Inner Disks have been assembled and commissioned.
- 2007-2012 Commissioning and running coordinator of CMS Tracker. He started to work to the R&D for the upgrades of the pixel detector with contribution to Lepix project and later to a hybrid solution for the pixel detector of CMS. He has been one of the editors of Pixel Upgrade TDR for the Phase 1.
- 2013: He has been nominated deputy coordinator for the CMS Tracker phase 2 upgrade, with responsibility of the pixel detector.

Natale Demaria is author or coauthor of more than 400 papers on international scientific journals and conference proceedings.

GIUBILATO Piero is a staff researcher and assistant professor at Padova University since 2012. His research interests cover the development of innovative pixel detectors for particle imaging and the realization of imaging/tracking system employed in high energy physics experiments as well as in applied sciences apparatus. He is an associated scientist at CERN since 2007, where he co-holds a patent on innovative monolithic pixel sensor architectures. As a visiting scientist at Berkeley Laboratory (2006 – 2010) he participated to the realization of the TEAM sub-angstrom electronic microscope, as well as to the development of counting imaging technique. As member of the CMS collaboration, he actively contributed to realization of the pixel tracker for the CMS experiment at the CERN LHC. Together with the development of new solid states sensors and imaging systems, he has long experience in radiation testing and assessment of integrated micro-electronic circuits, a field where he contribute to the realization of the IEEM nuclear microscope, the first instrument able to micro-map Single Event Effects in microelectronic circuits with unfocused ion beams.

BECCHERLE Roberto Degree in Physics in 1993 at University of Ferrara; PhD in Physics in 1997 at University of Padova; since 1999 Technical Researcher at INFN.

- in Genova INFN, he contributed to the development of the Module Controller Chip for the ATLAS Pixel Detector, in 0.25um IBM technology. Particular effort went in developing a RadHard resistant architecture and design. He also developed custom serial link protocols for configuring and reading out the chip, together with complete event building. The chip is currently installed in the ATLAS Pixel detector.

Starting in 2008 worked on FE-I4 ATLAS Pixel chip in 0.13um IBM technology. Chip will be used in the Insertable B-Layer for ATLAS phase1 upgrade.

Since 2011 he is working at INFN in Pisa to the FastTrack Associative Memory chip in CMOS 65nm TSMC technology.

RIVETTI Angelo: earned his diploma degree (Laurea) in Physics from the University of Torino in 1995. In February 2000 he obtained a PhD from the Polytechnic school of the same city, defending a thesis on the design of radiation tolerant analog a mixed signal circuits in deep submicron CMOS technologies. After a period as research assistant with the University of Torino, he joined INFN as a permanent staff member, where he is current a senior researcher.

- He has developed front-end electronics for the ALICE and COMPASS experiments at CERN and has worked at the R&D for hybrid pixel detectors for the PANDA and NA62 experiments.

- Current research interests: the design of front-end electronics for radiation sensors in ultra-deep submicron CMOS technologies, monolithic pixel sensors and very high accuracy timing circuits.

He has authored or co-authored more than fifty papers in the field of electronics for radiation sensors. He is the organizer of the 2011 and 2013 edition of the short course on front-end electronics at the IEEE NSS-MIC conference.

LIBERALI Valentino: Laurea degree in Electronic Engineering in 1986 from the University of Pavia, Italy.

He is now an associate professor of Electronics with the Department of Physics of the University of Milan.

- Main research interests: the design of mixed-signal circuits, analog/digital interfaces, sensor interfaces, radiation-tolerant IC design, and ASICs for high energy physics.

- Responsible of the Milan unit in the SkyFlash 262890 FP7 Project, aiming at developing a strong rad-hard-by-design (RHBD) methodology for the realization of non volatile flash memories based on standard CMOS processes.

RE Valerio: degree in Physics with Laude on 1985 at University of Milano; Ph.D. in Electronic and Computer Engineering on 1990 at University of Pavia. Post-doc on 1991 and Assistant Professor on 1992 at the University of Pavia. Associate professor on 1998-2006 and full professor of Electronics since 2006 at the University of Bergamo.

- Research interests: design of analog devices and front-end circuits for radiation detectors; study of noise and radiation effects in electronic devices; development of electronic instrumentation for the characterization of solid-state devices; nanoscale CMOS technologies for IC; monolithic active pixel sensors in CMOS technologies in the 100-nm regime.

- Principal Investigator of the INFN project VIPIX on pixel sensors in 3D microelectronic technologies.

- Since 2011 co-coordinator of WP3 in the AIDA EU-project. Main goals are: 3D technologies between microelectronic circuits and high-resistivity semiconductor sensors; creation of a common library of IP blocks in 65 nm CMOS.

Joined CMS experiment at LHC in 2013, with main interest on the Phase II upgrade of the Tracker.

He is author or coauthor of more than 200 papers on international scientific journals and conference proceedings.

1.6 ABSTRACT

Technology innovation in electronics has always been a fundamental step towards the conception of new experimental techniques in HEP or the achievement of unprecedented performance on known detectors. The front-end electronics is a fundamental part of the system, and fulfils the task of collecting, amplifying, storing and processing the signal coming from the sensor and reading it out to the back-end electronics for further treatment. Steps in electronics technology are important for making smarter and faster detectors, implementing new capability and/or allowing them to work in more harsh conditions where previously it was impossible to operate.

Running HEP detectors have front-end electronics based on CMOS 0.25 μm technology, and recent upgrades or new projects are very often using CMOS 130nm technology. The High Energy Physics community is now starting to invest on CMOS 65nm technology. There is already a project making use of 65nm technology on the back end electronics, the FTK project of ATLAS, but the use for front-end electronics is still at the very early start.

The CHIPIX65 project has the purpose of exploiting the CMOS 65nm technology on the very front-end electronics for use at future colliders, building core elements in digital and analog electronics and understanding and solve chip integration issues that are particularly important when a sophisticated chip digital circuitry, with an unprecedented amount of transistors, has to be integrated with the very front end analog electronics. Moreover, the radiation hardness of the technology has to be characterized and understood, in particular studying how the performance of electronics are modified, and special circuitry has to be developed to cope with Single Event Upset.

We have decided to choose a heavily focused R&D in order to have clear goals and deliverables and an evaluation of the final achievements, implementing the technology on a detector of great interest for the HEP and the INFN, where the requirements on the front end are pushed to the frontier.

Pixel detectors, in the last decade, have been technology drivers in HEP, having to integrate sophisticated electronics in a small space, coping with high data rates per unit area and a very granular sensor. In particular LHC experiments are strongly relying on pixel detectors for resolving the tracks elements in the very crowed volume around the interaction point. Future upgrades of LHC are pushing further the requests on a pixel chip. The challenges include: smaller pixels to resolve tracks in boosted jets, much higher hit rates (1-2 GHz/cm^2), unprecedented radiation tolerance (10 MGy), much higher output bandwidth, up to few Gb/s, and large IC format with low power consumption in order to instrument large areas while keeping the material budget low.

CHIPIX65 project goal is the The goal of this three years project is the development of an innovative CHIP for a PIXel detector, using a CMOS 65nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. New circuits will be built and characterized, a digital architecture will be developed and eventually a final assembly of a first prototype will be made.

Seven INFN units are participating to the project, with 35 members experts on the field, of which 20 are actual VLSI designers, constituting a substantial fraction of INFN expertise on microelectronics. This makes CHIPIX65 a unique opportunity for an efficient propagation across INFN of CMOS 65nm technology and constitutes the greatest collaboration on a microelectronics project ever made across INFN.

1.7 Background Intellectual Property Rights (BIPR)

Background Intellectual Property Rights are: Information & knowledge (including inventions, databases, etc.) held by participants prior to their accession to the Grant Agreement of a project.

CHIPIX65 will follow the basic rule that is: Intellectual property generated during a project remains the property of the participating organizations.

Discussions among CHIPIX65 and RD53 collaboration will be taken in order to establish a common sharing of BIPR.

1.8 PROJECT IMPLEMENTATION

CHIPIX65 is organized in the following Work Packages (WP), identifying four strategic branches of the project.

Work Package	Leaders	Unit
WP1: RADIATION HARDNESS	GIUBILATO Piero	Padova
WP2: DIGITAL ELECTRONICS	BECCHERLE Roberto	Pisa
WP3: ANALOG ELECTRONICS	RIVETTI Angelo	Torino
WP4: CHIP INTEGRATION	RE Valerio LIBERALI Valentino	Pavia Milano
WP5: PROJECT MANAGEMENT	DEMARIA Natale	Torino

Table 3: WP organization

1.8.1 WP1 Radiation Hardness

Aim of the CHIPX65 proposal is focused on the design of a hybrid pixel read-out chip for the rate and radiation expected in the ATLAS and CMS Phase 2 upgrades. In particular the chip must work reliably in an unprecedented radiation environment of 10 MGy Total Ionizing Dose (TID) and 10^{16} n.eq./cm^2 in 10 years. Acquired pixel information must be processed and stored reliably in such hostile radiation environment. A

dedicated effort is needed to investigate such high radiation tolerance and this will be a central concern of the Collaboration.

The chosen CMS 65nm technology has shown to be more radiation hard than 130nm, but it has been tested only up to 3 MGy. Moreover, the role of time delivery of the total dose and possible annealing effects should be understood, together with a temperature dependency. The program of the characterization of the radiation hardness of this novel technology has to be continued further for understanding its use in the front end of pixel detectors, and it is the purpose of WP1 of CHIPIX65 program.

Characterization is not limited to single transistors but covers the whole logic cell library. One can expect several digital storage elements (e.g. pixel data, configuration data, state machines) on the chip will have its content corrupted by radiation induced Single Event Upsets (SEU) every second.

Modified transistor simulation models must be extracted to allow the degradation to be taken into account during the design phase. This might require the creation of a full custom logic cell library.

On the contrary CMOS transistors are normally very resistant to Total Displacement Damage (TDD) but this has never be verified at this huge fluence values. Bipolar devices used in certain basic reference blocks will most likely become so affected that alternative circuits have to be developed.

Characterization of the technology at the required radiation levels is of fundamental importance for the experiment. The following measurements will be done:

1.TID effects on test structures and then on transistors at standard, reference, X-ray machine. Dependence of the damage from dose rate will be studied along with the presence of annealing effects and their dependence from temperature. In addition, to reduce the long irradiation times needed at the X-ray machines to attain 10 MGy, alternative radiation sources, as low energy electron linacs, will be investigated.

2. TDD effects by exposing test structures to proton and neutron beams. TID and TDD interplay will be analyzed also by comparing results from different subsequent irradiations with X-rays and neutrons.

3. Sensitivity to SEE, in particular to SEU (Single Event Upsets) and SET (Single Event transient), of logic cells with ion beams.

The technology characterization to TID and TDD will start immediately using test structures already available at CERN. Characterization of transistors developed within the Collaboration will follow, as soon they will become available.

Sensitivity to SEE of logic cell arrays will be performer in the second year and will extend in the first part of the third year. Measurements could include micro-mapping of the sensitivity.

1.8.2 WP2 Digital Electronics

Fault tolerant chip architectures will be explored, developed and simulated using the HDVL (Hardware Description and Verification Language) System Verilog at both architectural level and logic level. Such tool, widely adopted for complex designs in industry, will be used for creating a dynamic and reusable verification and simulation environment. The performance of alternative pixel readout chip architectures will therefore be analyzed at increasingly refined level as the design progresses. Architectures will be gradually optimized for minimal power consumption and very compact layout area to accommodate required digital signal processing and buffering functions. In order to do this they will feature group of pixels (i.e. pixel regions) that share buffering logic; one critical aspect of such strategy is the number of pixels to put in a single pixel region and the communication between them.

Independently of the actual pixel chip architecture implementation and optimization, a number of vital generic functions are required for a complete ASIC system. Despite that such functions (generally called IP blocks) are relatively common functions found in modern commercial integrated circuits, they have to be designed and optimized specifically for the pixel application because of the very hostile radiation environment with significant TID effects on the basic transistors and radiation induced single event upsets. Together they represent a large design effort, but one that ideally lends itself to be shared among collaborating groups. Typically each of these blocks will be designed by a single designer or team at a single institute.

1.8.3 WP3 Analog Electronics

Different low noise and low power analog circuit architectures and implementations will be developed for the critical amplification of the small pixel signals followed by appropriate signal shaping. Very low power digitization schemes based on time over threshold (ToT) and successive approximation ADCs will be evaluated and one of them will be implemented and optimized for massively parallel use in a large pixel chip.

Biasing circuits, charge sensitive amplifiers, discriminators, clock regeneration circuits; will be designed for use in very high level radiation environments. Circuits for fast readout and high-resolution time measurements for high rate pixel detectors like Phase Locked Loops (PLL) and timing measurement circuits will be developed.

All developed circuits will be implemented and prototyped in MPW runs of a 65nm CMOS technology and extensively characterized from the standpoint of analog performance and of radiation effects.

1.8.4 WP4 Chip Integration

This Work Package will take care of the global design of the pixel readout chip, from the definition of the architecture and floorplan, to the implementation of a common environment for simulation and verification.

The activity of WP4 is even more crucial in the case of a 65 nm CMOS integrated circuit than it already was for previous chip generations in former technology nodes. The greater complexity of design tools, along with the increased integration density, foster the need of tackling many issues at a global system level, taking into account that low-noise, high-accuracy analog blocks will be merged into a mostly digital environment.

In a first stage of the work, WP4:

- will cooperate with the other WPs and with other RD53 groups to define requirements and specifications of the readout chip. On the basis of these specs, WP4 will collaborate to the study of the architecture for the data readout of the pixel matrix. This preliminary stage will be essential to understand how some critical parameters should be kept under control in the global chip design, to avoid a degradation of the performance of analog and digital cells.
- will take care of the definition of a common CAD platform and standard formats for design information exchange, and will coordinate the definition of design guidelines for power grid, clock tree, and signal interfaces between different blocks (e.g., for hard blocks: LEF files for geometry; Liberty files for timing/power). Pad rings structure, use of standard cells provided by the foundry, and number of routing levels shall be defined at the beginning of the project.

In a second stage of the project, WP4 will provide an analysis of design solutions to the diverse issues that are crucial for the correct operation of the chip. These are just some of the problems that WP4 will tackle:

- Since the power dissipation of the chip will have to be kept under control even considering the huge amount of digital data flow, we will study possible techniques for distributing clock signals to the pixels and for transmitting and receiving data on- and off-chip in a low-power fashion. This may involve the use of non-standard digital levels and the consequent need for appropriate regeneration circuits.
- Distributing power supplies to a large pixel matrix may be critical, since even small voltage drops along power lines may affect the performance of analog circuits and cause a non-uniform behavior of pixel readout cells in different matrix regions. Techniques for the mitigation and compensation of power supply drops will be devised and implemented by WP4 in the global chip design. On-chip power conditioning and regulation is also crucial, and WP4 will study the performance of voltage regulators and DC-DC converters that are being developed by the community working on 65 nm CMOS.
- Digital-to-analog interferences might impair the detection of small signals in analog cells and induce fake hits. WP4 will define the best design strategy to prevent these effects to occur in a unacceptable way.
- The chip will contain a complex analog and digital system that needs to be monitored and calibrated in an accurate way. WP4 will study the integration in the chip of temperature monitoring ADCs, voltage calibration DACs, circuits for the injection of analog test signals in the pixel cells, PLLs for

the regeneration of external clock signals, and so on. Some of these blocks may be developed by the community that is starting to create a common library of IP blocks in the 65 nm technology. WP4 will monitor these developments and contribute to them when this will be needed for the design of the pixel readout chip.

These design solutions will be at least partially tested in the chip prototypes that will be submitted by CHIPIX65.

In a third stage of the project, WP4:

- will accomplish the task of designing the final demonstrator chip, by integrating the blocks designed during the project. Analog and digital pixel cells will be integrated together in the global chip environment.
- The work will culminate in the final CHIPIX65 submission, for which WP4 will take care that the various groups will share circuit blocks and design tools in the most effective way. The final verification steps and the submission of the design will be carried out under the responsibility of WP4.

1.8.5 WP5 Project Management

CHIPIX65 project is composed of 7 research units and 35 members. The research program has to be organized in a proper and effective way and efficient communication has to be maintained across the whole project, all this in a pragmatic and simple way. For that reason a Steering Board and an Institute Board are needed, one representing the lead of the scientific activities and the other representing all the research units. The Steering Board will have regular short meetings, of the order of one per month, making a review of the activities and taking decision when needed. The Steering Board will be composed by the WP leaders and by the Project leader that will be the chair. Minutes will be produced and will be distributed to all CHIPIX65 members. The Institute Board will be formed by all responsible of the research units and will meet at least once or twice per year, or when needed.

The project leader is responsible of the entire project. The WP leaders are responsible for the deliverables under their WP, and should take care of the organization and distribution of the work, of keeping good communication across the whole CHIPIX65, starting from the Steering Board to the members. The unit responsible should oversee the activity made in their units and to represent all their members in CHIPIX65.

CHIPIX65 will have a common meeting once or max twice per year of about one day with at least one report per WP activity and one report per single institute. Details of the meeting will be decided by the Steering Board and with the approval of the Institute Board.

1.9 PROJECT TIMELINE

WP	No	Activity	start	end	Deliverable
1	1.1	Basic radiation test structure	2014-Q1	2014-Q2	Report
	1.2	Basic radiation test structure: MPW design	2014-Q2	2014-Q3	MPW 1
	1.3	Basic radiation test chip test results	2014-Q4	2015-Q1	Report
	1.4	Complex radiation test structures MPW submission (gates, flip-flops, memories)	2015-Q1	2015-Q3	MPW 3
	1.5	Complex radiation test chip test results	2015-Q4	2015-Q3	Report
	1.6	Qualification of technology to 10 MGy TID, 10^{16}n/cm^2	n.a.	2015-Q4	Milestone
2	2.1	Digital logic definition and requirements	2014-Q1	2014-Q2	Report
	2.2	Digital basic IP blocks: design	2014-Q1	2015-Q2	MPW 3
	2.3	Digital basic IP blocks: testing	n.a.	2015-Q3	Milestone
	2.4	Digital architecture: evaluation of different schemes	2014-Q1	2014-Q4	Report
	2.5	Digital architecture: pixel/region basic model in	2014-Q1	2015-Q1	Report

		SystemVerilog			
	2.6	First Digital pixel region with some Analog Pixel to study A/D cross-talk: design	2014-Q1	2014-Q4	MPW 2
	2.6	Digital architecture simulation model	2014-Q1	2015-Q2	Report
	2.7	Digital architecture: pixel region design submission with small pixel array	2015-Q2	2015-Q4	MPW 4
	2.8 / 1.7	Measurement with ion beams of SEU rate in digital cells		2015-Q4	Milestone
	2.9	Definition of Digital Architecture of Prototype			Milestone
	2,10	Digital architecture model highly optimized for fault tolerance and low power	2015-Q3	2016-Q4	Report
3	3.1	Mixed A/D signal blocks definition/requirements	2014-Q1	2014-Q3	Report
	3.2	Analog basic IP blocks: design	2014-Q1	2014-Q3	MPW 1-3
	3.3	Test of first Analog Blocks and VFE chain	n.a.	2014-Q4	Milestone
	3.3	Definition of VFE architecture	n.a.	2015-Q3	Milestone
	3.6	Mixed signal blocks functional and radiation test results	n.a.	2016-Q1	Milestone
4	4.1	Requirements and specifications of pixel readout chip. Definition of common formats and interfaces between different blocks	2014-Q1	2014-Q3	Report
	4.2	Design methodology & verification of $5x10^8$ transistor IC	2014-Q1	2015-Q3	Report
	4.3	Analog integration in large digital chip, power distribution	2014-Q1	2016-Q4	Report
	4.4	Synthesis constrain, clock distribution and optimization			Report
	4.5	Ready for Chip integration of Prototype		2015-Q4	Milestone
	4.6	Final chip prototype design in 65 nm and submission to the foundry	2016-Q1	2016-Q3	Submission
	4.7	Final Report	2016-Q3	2016-Q4	Milestone

Table 4: CHIPIX65 Timeline

WP	No	Activity	2014				2015				2016			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
1	1.1	Basic radiation test structure												
	1.2	Basic radiation test structure: MPW design												
	1.3	Basic radiation test chip test results												
	1.4	Complex radiation test structures MPW submission (gates, flip-flops, memories)												
	1.5	Complex radiation test chip test results												
	1.6	Qualification of technology to 10 MGy TID, 10^{16}n/cm^2												
2	2.1	Digital logic definition and requirements												
	2.2	Digital basic IP blocks: design												
	2.3	Digital basic IP blocks: testing												
	2.4	Digital architecture: evaluation of different schemes												
	2.5	Digital architecture: pixel/region basic model in SystemVerilog												

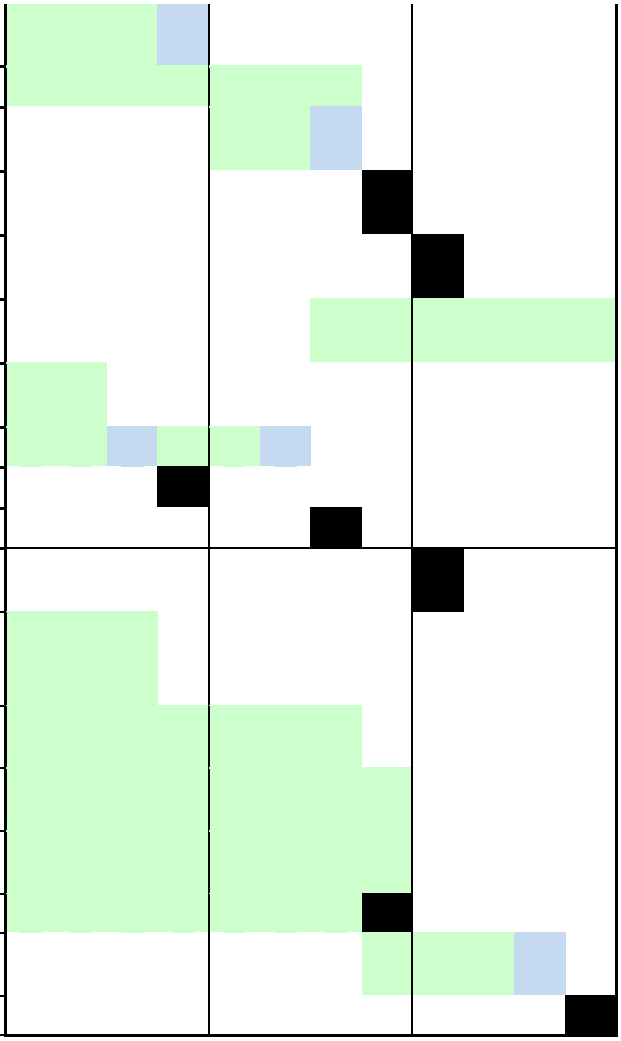
	2.6	First Digital pixel region with some Analog Pixel to study A/D cross-talk: design	
	2.6	Digital architecture simulation model	
	2.7	Digital architecture: pixel region design submission with small pixel array	
	2.8 / 1.7	Measurement with ion beams of SEU rate in digital cells	
	2.9	Definition of Digital Architecture of Prototype	
	2,10	Digital architecture model highly optimized for fault tolerance and low power	
3	3.1	Mixed A/D signal blocks definition and requirements	
	3.2	Analog basic IP blocks: design	
	3.3	Test of first Analog Blocks and VFE chain	
	3.3	Definition of VFE architecture	
	3.6	Mixed signal blocks functional and radiation test results	
4	4.1	Requirements and specifications of pixel readout chip. Definition of common formats and interfaces between different blocks	
	4.2	Design methodology & verification of $5x10^8$ transistor IC	
	4.3	Analog integration in large digital chip, power distribution	
	4.4	Synthesis constrain, clock distribution and optimization	
	4.5	Ready for Chip integration of Prototype	
	4.6	Final chip prototype design in 65 nm and submission to the foundry	
	4.7	Final Report	

Table 5: CHIPIX65 Timeline, graphical display

1.10 FINANCE REQUEST

In the following Table is described the overall cost of the CHIPIX65 project, detailed for different chapters.

TYPE of COST	TOTAL COST
MISSIONI	
Irradiation and Testing	21
Work among IC designers	21
1 CHIPIX65 meeting per year	9
Conferences	13
CONSUMI	
Small Board for analog testing	13
Low Level chip characterization test system	105
Irradiation consumable	20
Submission to Foundry	580
INVENTARIABILE	
Consolidation PC Cluster for Chip	30

Integration, verification and simulation (analog and digital)	
OVERALL TOTAL	**812**

Table 6: Finance Request of CHIPIX65 for the three years (2014-16)

1.10.1 Participation of RD53 collaboration

Most of the research units of CHIPIX65 are also member of the international collaboration RD53 that has been approved recently by the LHCC committee. The following institutes are participating in RD53: from ATLAS: Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, UC Santa Cruz; from CMS: Bari, Bergamo-Pavia, Fermilab, Padova, Perugia, Pisa, PSI, also RAL, Torino; from both: CERN (also on CLIC) and RAL. There are 99 members of which about 50% are chip designers. The purpose of the RD53 is the development of pixel readout integrated circuits for extreme rate and radiation.
RD53 does not provide financial support for the defined R&D activities. It will be based on contributions from each institute/country, provided by the national funding agencies.
The interest of CHIPIX65 institutes to be in RD53, or to work together with, is that it provides the collaboration framework to enable synergies at international level, sharing experience with worldwide HEP experts in the field and focused on this common interest. It will also allow to reach the best sub-division of work among participating members to guarantee the success of the defined R&D project.

CHIPIX65 will make the contribution of the INFN groups stronger and self-consistent inside such an international R&D activity. This assures to maximize the overall results and experience obtained by the CHIPIX65 units in the context of using modern radiation tolerant CMOS technologies for front end electronics and in particular for future generation pixel chips required for the HL-LHC.

2 SCIENTIFIC PROPOSAL

2.1 State of the art

Hybrid pixel ASIC's in the current LHC experiments can sustain pixel hit rates of up to 200 MHz/cm^2 with an effective resolution of the order of ten microns. An extensively used CMOS 250nm technology employing a special layout approach (enclosed transistor layout) has been used to implement pixel chips that can survive radiation levels of up to ~1MGy and ~10^{14} neutrons/cm^2. For comparison, radiation tolerant ASICs used for space applications can only work at radiation levels up to ~1kGy.

Recent pixel developments based on CMOS 130nm technology are Medipix and Timepix, ToPix and the FE-I4 chip of the ATLAS collaboration. The latter has been specified to meet more extreme conditions foreseen for the closest future upgrade of LHC (so called Phase 1 upgrade, from 2018). We can consider the FE-I4 a second-generation LHC pixel detector. The FE-I4 improves upon the current ATLAS pixel detector in terms of 40% smaller pixel size, a factor of 5 higher hit rate, die area devoted to periphery of 10% instead of 30%, full reticle die size (to minimize bump bonding cost), and higher radiation tolerance (requirement of 3.5 MGy). Important advances of FE-I4 include the use of commercial logic cells fully synthesized as part of the pixel matrix, and a so-called "region" readout architecture which combines all digital processing from every group of 4-pixels into one synthesized logic block. This block performs the analog to digital conversion, hit storage, and time look-back retrieval functions previously relegated to the chip periphery. Thus about half the area and the great majority of the transistors within the pixel matrix consist of synthesized logic, permitting a small periphery. Placing most digital processing within the pixel matrix allows sustaining higher hit rates while reducing digital power, because most hits are held within their respective region until the trigger latency expires, and then erased, with no need for high data bandwidth between pixels and periphery. The price of local digital processing is that digital noise is injected into the analog front end. Power distribution and substrate isolation options available in the 130 nm CMOS process were critical to achieve these goals, as were the excellent digital design tools available for modern processes.

2.2 Challenge of the proposal

A new pixel detector will be needed for ATLAS and CMS for the HL-LHC period, where the instantaneous luminosity will be five times the present one, and twice that of Phase 1, reaching 5 10^{34} cm^{-2}s^{-1}, and determining a pile-up of at least 100 in the scenario of 25 ns bunch crossings, and an integrated luminosity of 270 fb^{-1} per year, therefore of the order of what will be collected in the entire Phase 1 period. The most important areas of improvement for the pixel detector that have been identified are:

- Increased radiation hardness of inner layers;
- Improved rate capability of the ROCs;
- Increased granularity, using smaller pixels;
- Implemented trigger functionalities.

A new pixel detector ASICs for hybrid pixel detector systems must be developed for the ATLAS and CMS detector upgrades to obtain improved spatial resolution to the few μm level at pixel hit rates up to 2 GHz/cm^2 and working reliably for ~10 years in extremely harsh radiation environments with up to ~10MGy total dose and 10^{16} neutrons/cm^2. Table 7 shows the main requirements for the new chip for phase 2 upgrade, compared with previous generation pixel chips: the challenge in performance from previous pixel chip generation is quite evident.

The 130 nm CMOS technology is currently used for several short-mid term pixel projects in the HEP community (ATLAS IBL, Medipix, LHCb VELOpix, etc.), and has been considered as a possible option for the high luminosity CMS pixel upgrade. It is however estimated not to offer sufficient logic density to fulfill all the requirements for a HL-LHC pixel upgrade.

The development of such a chip requires a real R&D effort using a higher integration scale VLSI technology. A workshop[1] was held at CERN in Nov 2012 to collect the experience from experts in the field from CMS /

[1] "ATLAS-CMS 65 nm pixel ASIC meeting," https://indico.cern.ch/conferenceDisplay.py?confId=208595 (2012)

ATLAS and other pixel projects/VLSI activities, interested to the development for HL_LHC. INFN was present with several experts and CMOS 65nm technology seems to be very promising.

PARAMETER or FEATURE	**1st generation LHC phase 0**	**2nd generation LHC Phase 1**	**3rd generation LHC Phase 2**
CMOS technology	250nm	250nm / 130nm	65nm
Max Particle Flux	~50 MHz/cm^2	~200 MHz/cm^2	~500 MHz/cm^2
Max Pixel Flux	200 MHz/cm^2	600 MHz/cm^2	2 GHz/cm^2
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 μm^2 50x400 μm^2	100x150 μm^2 50x250 μm^2	25x150 μm^2 50x100 μm^2
Signal Threshold	2500-3000 e$^-$	1500-2000 e$^-$	~1000 e$^-$
L1 Trigger Latency	2-3 μs	4-6 μs	6-20 μs
L1 Trigger Rates	100 KHz	~100 KHz	200-1000 kHz
L1 Trigger contribution	no	no	clustering info @L0 self-triggering
ASIC side	~1 cm^2	~4cm^2	1-4cm^2
Hit memory per chip	0.1 Mb	1 Mb	~16 Mb
Chip output bandwidth	~40 Mb/s	~320 Mb/s	~3 Gb/s
Power Budget	~0.3 W/cm^2	~0.3 W/cm^2	<0.4 W/cm^2

Table 7: Evolution of Main requirements of Pixel detector at LHC among generations

The choice of IC technology is a delicate decision of utmost importance for such a long term and challenging project. Tolerance to the unprecedented radiation level is one of the prime drivers, but the technology must meet several other specific requirements, which we believe are met by the CMOS 65 nm node:

- Appropriate for highly integrated analog/digital mixed signal designs
- Sufficient circuit density for both analog and digital functions
- Low power consumption
- Well defined and reliable design kit for complex modern technology
- Flexible access by the HEP community
- Affordable for small prototype circuits and for the very large final pixel chips, and finally
- Long term availability from multiple vendors, as qualification, design, prototyping, testing and final production will stretch over a relatively long period of 5-10 years.

CHIPIX65 project has as one main goal that of promoting inside INFN the use of the novel CMOS 65nm technology for the front-end electronics, focusing the effort on a first 65nm prototype chip for the use at HL_LHC pixel detectors. The final chip for the ATLAS and CMS experiments will be continued after this R&D phase and CHIPIX65 will allow INFN to play a leading role in those efforts in the two communities.

The chosen 65nm technology has so far been extensively radiation tested up to a total dose of 3MGy with very promising results. For the Phase 2 pixel projects the inner pixel layer this characterization needs to be extended to 10MGy. Initial, but very preliminary, indications have shown that certain P-MOS transistor parameters may experience a significant degradation above the 3MGy level. These studies need to also be extended as a function of temperature. Significant additional work is required to develop an understanding of such effects. In addition to single transistors, characterization must be extended to logic cell libraries. Depending on the 65nm CMOS technology the final qualification of an appropriate technology for extremely harsh radiation environments is not yet finalized, so a direct collaboration with a particular IC foundry has not yet been fully established. Initial testing of 65nm technologies from ST and TSMC indicates that both

technologies have promising radiation tolerance.

Pixel chips are very complex low power mixed signal integrated circuits with an extremely tight integration of low noise analog circuits and complex digital functions. The very small analog signals from the pixel sensor array must be captured and amplified in each individual pixel by very low noise charge integrating preamplifiers, shaped to appropriate pulse shapes and finally digitized for further digital processing. The very large number of pixels in a pixel chip (100k – 1M) makes the analog circuit design particular critical for physical layout area and for very low power consumption. Matching of critical analog performance parameters across so many channels over large chips is another particular challenge when using modern deep sub-micron IC technologies. Novel digital architectures must be developed to cope with the required on-chip digital signal processing, data buffering and readout with low power consumption and being immune to radiation induced single event upsets (SEU rate per chip: ~10 random bit flips per chip per second).

Very low power and very small area circuit implementations for the required digital logic per pixel cell and per pixel region (e.g. 4x4 pixel cells) will be explored, developed, simulated and implemented in a 65nm CMOS technology prototype chip. Different approaches to achieve radiation tolerance to the 10MGy level and SEU immunity in critical functions will be evaluated. Alternative logic architectures (gated clock synchronous, asynchronous, dynamic logic, etc.) will be evaluated and compared and the most efficient will be implemented in a pixel array chip in a MPW. The prototype chip will be characterized and tested for correct function and low power consumption during exposure to very high radiation levels.

Digital memory structures in 65nm CMOS will be optimized at the circuit and layout level. The detailed mechanism of localized charge deposits from particles in the layout structures of the 65nm technology will be studied to propose and implement memory structures with significantly decreased single event upset cross-section. Dedicated full custom layout implementations of latches, flip-flops and RAM will be prototyped in MPW runs and extensively tested for improved/decreased SEU sensitivity. The mechanism behind multiple bit upsets will be studied and schemes to prevent this will be proposed and tested in prototype circuits.

As mentioned above, to handle such high data rate the hit information can be stored locally within the array as shown in Fig. 1. Storing information from multiple hits from the same cluster together translates into significant savings in required storage resources. Sharing of latency buffers in particular leads to compact circuitry and low power. The exact way in which the hit data are stored must be optimized for the new requirements and technology. What this means in practice is understanding how many pixels share storage logic (so-called regions), in what pattern, with what internal organization, and how are region boundaries handled. FE-I4 uses 2-by-2 pixel regions that were the results of an optimization carried out for that design.

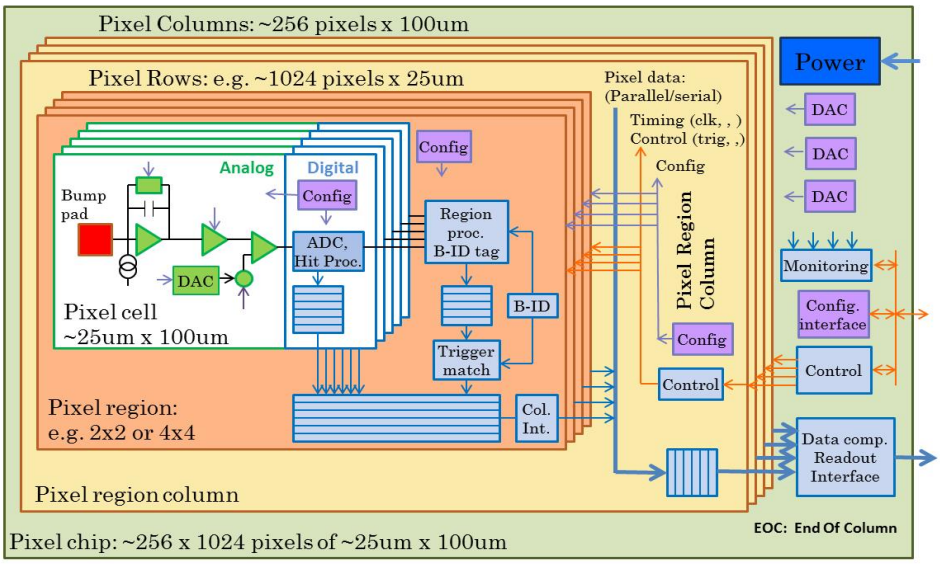


Figure 1: Diagram of pixel hierarchical organization and architecture

This optimization does depend on cluster size distributions, which in turn depend on sensor type and location in the detector, and on physics input. It is also necessary to consider the grouping of the sensitive analog

circuits into well-isolated “analog islands”, which will depend on the process options and on how power is distributed within the chip.

To effectively perform such complex optimizations at all levels of the architecture, a dedicated pixel simulation and verification platform will be an indispensable development tool. This platform must be capable of simulating alternative pixel chip architectures at increasingly refined level as the design progresses. Automated verification functions must be part of such a framework to enable extensive simulations of large sets of pixel hits and triggers to be performed in an automated fashion for global architecture evaluations and for all incremental extensions and refinements of a final design. Large data sets of realistic (and extreme) pixel hits and triggers can be generated with given constrained random distributions within the framework. Particle hits from external full detector/experiment Monte Carlo simulations and detailed sensor simulations can be imported and mixed with statistically generated hits. A simulation and verification framework tailored for the high rate pixel detectors for the ATLAS/CMS upgrades could also be a highly valuable tool for other HEP pixel detector systems and ASICs in general. The framework will be developed using the HDVL System Verilog and the UVM (Universal Verification Methodology) library.

2.3 SCIENTIFIC INNOVATION AND INTEREST FOR INFN AND CNS5

CMOS 65nm technology is being used extensively for industrial and automotive applications that require availability over extended periods. Nevertheless the HEP community has little or no experience with it on the front-end electronics, while has already started its use in the back-end with the FTK project. It is of outmost importance that INFN has a leading role in the use of this new technology, that will open up new possibilities with implementation of local intelligence in the front-end, with low noise performance, and all this will make it possible to reach unprecedented performance in several detection systems. Boosting the technology innovation inside the INFN is of course one of the main goals of CSN5, where the CHIPIX65 find its natural collocation.

The CHIPIX65 project is serving the purpose of pushing the use of CMOS 65nm in the INFN across a wide community of IC designers that are spread across several INFN divisions. The choice of a focused R&D is to have a clear use-case and a clear deliverable with milestone and time schedule, not imposed only by the three years term of the project itself, but by the scientific program of an international community of the LHC experiments.

Key research and development domains of this proposal are:

· Low noise, low power analog design.

· Novel low power analog to digital conversion for small dynamic range.

· Large mixed signal application specific integrated circuits.

· Massively parallel low power analog and digital architectures.

· Low power high speed readout circuits.

· Radiation test and qualification to very high radiation levels (of 65nm technology)

· Radiation hard design techniques

· Fault tolerant digital architectures, logic and circuits

2.4 ROLE OF RESEARCH UNITS

2.4.1 Bari

The unit of Bari will work mainly in the development of analog and digital IP blocks to be included in the common library available to the collaboration (WP2 and WP3). The analog blocks,like ADCs, DACs, I/O cells and bias circuitry will be designed and characterized considering the expected high radiation doses and minimizing the power consumption. The digital blocks will be designed using technics of SEU mitigation in which the Bari group has pasted experience. Different architectures of slow control and data readout will be

investigated and proposed. The design will be developed through synthesis, place & route and verification phases. Following the submission of MPW, the circuits will be qualified for their functionalities and radiation resistance.

2.4.2 Milano

The unit of Milano has designed ICs in 65 nm CMOS technology since 2010 within the FTK project, and has expertise in chip-level integration mixing different design approaches (standard-cell and full-custom design).

Moreover, Milano has a long expertise in radiation hardening by design (RHDB) techniques. The contribution of the Milano unit will be on the definition of common interfaces between circuit blocks, on RHDB at chip level, and on design and verification of the final chip.

2.4.3 Padova

The interests of Padova group lie within WP1 and WP4. By more than 20 years the Padova group is involved in the characterization and modeling of radiation effects on semiconductor detectors and electronic devices and systems. Irradiations are usually performed at facilities the group has built and operates: SIRAD at the Tandem accelerator (protons and heavy ions), X-ray machine and Co60 cell, all at the INFN Legnaro Laboratory. Consolidated collaborations allow easy access to reactor neutrons in Lubiana and to electron beams in Bologna.

The group has contributed in the past to the transfer of the APV chip, the front-end chip of the silicon tracker of CMS, from the original Harris rad-hard technology to the CMOS 250 nm one. The present contribution within WP4 concerns the design of analog IP blocks, as PLL and DC-DC converters.

2.4.4 Pavia

The INFN Pavia group has a wide experience in the field of the characterization of nanoscale CMOS technologies in view of the implementation in low-noise, rad-hard analog front-end circuits. Within the WP1, the Pavia group will study the radiation hardness of the 65nm CMOS technology through electrical (in particular noise) characterization of purposely designed test structures up to very high total integrated doses. The irradiation campaign will be performed at room temperature and/or at low temperature (-10 ÷ -20°C). In the framework of the WP3 activities, the Pavia group will design and qualify some individual rad-hard microelectronic blocks, which are needed in complex readout chips. The circuits that will be designed are as follows (but are not limited to): band-gap references, digital-to-analog and analogue-to-digital converters, I/O blocks composed of sLVDS-to-CMOS and CMOS-to-sLVDS transceivers. Moreover, the group will collaborate with other INFN units to the choice and the design of the analog processing chain (preamplifier, shaper, discriminator, ADC) of the pixel. Finally, the Pavia unit will contribute to the chip integration together with Milano, Torino and Pisa groups.

2.4.5 Perugia

The activity that the unit of Perugia intends to carry out in the framework of WP2 regards the development of functional blocks to be used in a devoted simulation environment. This environment will be used to analyze the operation and performance of alternative digital architectures of the readout pixel chip. The activity will be performed by using high-level modeling tools (SystemVerilog) in order to collect sufficient statistic on the actual performance of the system in very high rate high energy physics experiments. Both stimuli (hits) derived from statistical modeling at the detector level (eg ATLAS / CMS) and data produced by Monte Carlo simulations with a high rate and with appropriate scaling factors will be considered in the analysis. The Perugia group intends also to take part in the WP1, by using the expertise and instrumentation gained from earlier activities in the AMS space experiment. In the framework of WP1 the Perugia group will collaborate with Padova in Total Ionizing Dose testing using the X-ray machine available in Perugia.

2.4.6 Pisa

The Pisa research unit will work on the digital architecture of the chip, focusing on how the chip could contribute to a Level 1 (L1) trigger. These will be studied for two configurations: the one using self pixel-

chip detected data patterns and the one where the region is identified by a pre-trigger (L0) region from outside of the pixel system (like for instance calorimeter primitives). Possible L1 trigger schemes are:

- Jet-Vertex identification, done assigning the vertex to each jet out of ~200 vertices/bunch crossing
- Tau to three prongs identification, which involves recognizing compatible pixel cluster inside a chip
- Match pixel hits with external calorimeters, in order to identify electrons using tracks from pixels.

Starting from physics requirements, we plan to evaluate the feasibility from a synthesis point of view. In particular, we plan to study the optimization of large pixel regions in order to share as much as possible local resources in order to be able to implement the complex data algorithms needed for L1 trigger. The emphasis in this respect is twofold. On one hand the design of "islands cores" of pixels (like e.g. 4x8) and the other one the design of an architecture that allows the communication between these island cores.

One critical aspect of this design phase will be the evaluation of the noise induced by the digital circuits to the analog blocks, in those pixel regions. Furthermore all tight constraints coming from low power, low noise, reduced cell size, clock distribution in an highly irradiated environment will have to be studied.

Another task will be collaborating on the chip validation using industrial standards like SystemVerilog, UVM. We will be helping in the development of a suitable design flow to allow chip sign-off using reproducible results based on standardized intermediate verification steps. This should ease the integration of the various design blocks during all chip design phases, which is one of the biggest challenges of a > 2 x 2 cm^2 chip.

Last, but not least, we will participate to the development of the Test System, which will have to be focused from the beginning towards ease of use, expandability and integration with respect to the CMS DAQ in order to allow a smooth transition from first prototype testing to final full scale chip characterization and commissioning.

2.4.7 Torino

The main role of Torino is the development of analog electronics and IP blocks like ADC, PLL, I/O and to characterize their radiation hardness. We will design, realize and test the analog electronic chain of the very front end that has to be of low power, very low noise and to be very small in order to fit into a very granular pixel chip and to sustain very high particle rate typical of HL_LHC. We will study very fast comparators in order to reach ~1000e^- in-time threshold, and different solution for the signal digitization: local ADC or ToT will be explored. Torino has a large experience in the realization of front-end chip for HEP experiments, in particular the realization for the drfit silicon chamber of ALICE ITS and for the pixel detector of PANDA experiment (ToPix).

2.5 INVOLVEMENT OF OTHER LINES OF RESEARCH

2.5.1 Involvement of INFN CSN1

The CSN1 involvement in the CHIPX65 project is visible looking to the Table 1: several members of CHIPIX65 are heavily involved into CMS and ATLAS experiments. On top of that, additional physicists of those CMS and ATLAS INFN groups are involved in the work for the HL_LHC upgrades, both on the development of pixel sensors, on the physics simulation studies or in the Pixel Phase 1 upgrades. Only in CMS there are about 25 full time equivalent dedicated to Phase 2 Upgrade in the years 2014-16, several of which are located in the same groups of CHIPIX65.

While the CHIPIX65 activities are targeting the most R&D oriented topics, that will be dominant in the coming next three years, interest and sharing of work will be found in people involved in CMS and ATLAS experiments. Once the CHIPIX65 program will end, the results achieved in the R&D will evolve towards the design of the final CMS and ATLAS pixel chips, with a couple of engineering run during 2018-19.

Other experiments to future colliders (like ILC) or development for future upgrades of existing experiments, will also profit from of the achievements on the CMOS 65nm technology made in a large community of IC designers of CHIPIX65.

2.5.2 Involvement of CERN

CERN, thanks to the micro-electronics department PH-ESE-ME, has recently finalized a market survey and tender to get appropriate access to a 65 nm CMOS technology from the TSMC-IMEC foundry in the form of a FSFC. TSMC (Taiwan Semiconductor Manufacturing Company) is one of the largest IC foundries in the world. IMEC, a well-known European IC research institute, has partnered with TSMC to provide access for European university and small business IC designers to TSMC fabrication facilities. The FSFC will assure reliable and affordable access to the chosen technology together with the required local support. It also gives access to regularly scheduled and relatively low cost Multi ProjectWafer (MPW) runs. This is vital for our community during the R&D phase where small test circuits must be produced to verify functionality, radiation hardness and low power consumption.

2.6 PROJECT IMPLEMENTATION

2.6.1 Research Unit expertise and infrastructure

2.6.1.1 Expertise

Fifteen years' expertise on R&D of innovative silicon detectors and front-end electronics: CMS, ATLAS, ALICE at LHC. Design of micro-electronics (analog and digital) for use in high energy physics as well as medical applications in CMOS technology 250nm and 130nm, and recently 90nm and 65nm. Realization of pixel chips for PANDA (ToPix), Super-B (SuperPIX0); work on APV25; work on FEI4 chip (130nm) on Associative Memory chip for FTK (65nm); work on 65nm CMOS.

The details of the experience of the INFN units can be found in the following list of publications.

2.6.1.1.1 Publications:

- P. Giubilato et al., "First results in micromapping the sensitivity to SEE of an electronic device in a SOI technology at the LNL IEEM", Nucl. Instrum. and Meth. A 658 (2011) 125-128
- M. Bagatin, A. Paccagnella et al ., "Neutron-Induced Upsets in NAND Floating Gate Memories," IEEE Transactions on Device and Materials Reliability, ISSN: 0018-9499, Volume 12, pp. 437 -444, Jun. 2012
- M. Bagatin, A. Paccagnella et al., "Proton-Induced Upsets in 41-nm NAND Floating Gate Cells," IEEE Transactions on Nuclear Science, Volume 59, pp. 838 -844, Aug. 2012
- M. Bagatin, A. Paccagnella et al., "High-reliability fault tolerant digital systems in nanometric technologies: Characterization and design methodologies," Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2012 IEEE International Symposium on, pp. 121-125, 2012
- V.Re, G.Traversi et al "Introducing 65nm CMOS technology in low-noise read-out of semiconductor detectors", Nucl.Instrum. Meth. A624 (2010) 373-378.
- V.Re, G.Traversi, M. Mangisoni "Perspective of 65nm CMOS technologies for high performance front-end electronics" Proceedings of Science, Vertex 2012 Conf., 026.
- A.Rivetti et al. "A 130 nm ASIC prototype for the NA62 Gigatracker readout; Nucl. Instrum. and Meth. A650, (2011) 115-119.
- A.Rivetti et al. "A CMOS 130nm silicon pixel detector readout ASIC for the PANDA experiment", JINST 7 (2012) C02015
- A.Stabile, et al. "The AMchip04 and the processing unit prototype for the FastTracker", JINST 7 (2012) C08007.
- V.Liberali et al. "Performance of the AMBFTK board for the FastTracker processor for the ATLAS detector upgrade", JINST 8 (2013) C0140140.
- R.Beccherle, V.Liberali, A.Stabile et al "Associative memory design for the fast track processor (FTK) at ATLAS", IEEE Nuclear Science Symposium Conference Record, 2012, Article number6154467, 141-146
- R.Beccherle, et al, "MCC: the Module Controller Chip for the ATLAS Pixel Detector" Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment
- R.Beccherle et al., "The FE-I4 pixel readout integrated circuit" Nucl.Instrum. Meth A636 (2011)

S155-S159
- S. Saponara, , G. Magazzu' et al. "Development, Design and Characterization of a Novel Protocol and Interfaces for the Control and Readout of Front-End Electronics in High Energy Physics Experiments", accepted on IEEE Trans. on Nuclear Science, to appear in Feb 2013
- F.Loddo, G.De Robertis "Design and submission of rad-tolerant circuits for future front-end electronics at S-LHC" Nucl.Instrum Meth. A612 (2010) 455-459.
- P.Placidi, G.M.Bilei, et al., "Advanced active pixel architectures in standard CMOS technology," IEEE Transactions on Nuclear Science, 52 (5) , (2005) 1869- 1872
- D.Passeri, P.Placidi et al. "An active pixel sensor to detect diffused X-ray during Interventional Radiology procedure," Journal of Instrumentation, vol. 7, Issue 04, pp. 1-12, April 10, 2012.
- M.Menichelli et al. "The Radiation Hardness Assurance Facility at INFN-LNS Catania for the Irradiation of Electronic Components in Air. IEEE TNS, vol. 57 (2010), p. 2074-2078, ISSN: 0018-9499
- A.Marchioro, P.Placidi et al. "The control system for the CMS tracker front end,"IEEE Transactions on Nuclear Science, vol. 49, Issue 3, pp. 846–850, June 2002.

2.6.1.2 Infrastructures

2.6.1.2.1 Ba, Mi, Pd, Pv, Pg, Pi, To

- VLSI micro-electronics laboratories with proven and well established experience in the design, test and validation of full chip of innovative micro-electronics front end.
- EDA CAD tools for the VLSI design (Cadence Combined IC & Systems Package, Mentor Graphics ICdesign) and for device simulation (Synopsys TCAD).
- Clean rooms for assembly, interconnect, characterize and qualify micro-electronics and silicon devices, with facilities for wire-bonding, wafer probing and test benches.

2.6.1.2.2 Pd

- X-ray and Co^{60} irradiation facilities at INFN Legnaro Laboratory (LNL) for TID effects studies
- protons at the SIRAD irradiation facility at the LNL Tandem+ALPI accelerator system for TDD effects studies
- ion beams at the SIRAD+IEEM irradiation facility at the LNL Tandem+ALPI accelerator system for SEE studies.

2.6.1.2.3 Pg

X-ray machine with dosimetric system for total ionizing dose measurements

2.7 International Collaboration

2.7.1 RD53 Collaboration

The RD53 collaboration, recently approved by LHCC, has been described in Section 1.10.1. The involvement of all the experts in within HEP community in the research program that is in common with CHIPIX65, is very important for the success of these three years R&D proposal.

2.7.2 LHC experiments

The CMS and ATLAS collaboration are starting from 2013 to strongly enhance the interest on the HL_LHC upgrades. In the framework of the experiments are easily found synergies with other institutes, for example providing services in facilities like test-beams, irradiation that can be of use for the CHIPIX65 work

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2.8 Work program, Finance plan

TYPE of COST	2014	2015	2016	TOTAL COST
MISSIONI				
Irradiation and Testing	7	7	7	21
Work among IC designers	7	7	7	21
1 CHIPIX65 meeting per year	3	3	3	9
Conferences	3	5	5	13
CONSUMI				
Small Board for analog testing	5	5	3	13
Low Level chip characterization test system	30	50	25	105
Irradiation consumable	10	5	5	20
Submission to Foundry	140	140	300	580
INVENTARIABILE				
Consolidation PC Cluster for verification and simulation	10	20	0	30
TOTAL	215	242	355	**812**

Table 8: CHIPIX65 Finance plan

2.9 RISK ASSESSMENT

The goal of the CHIPIX65 project to realize electronic circuits in CMOS 65nm for innovative front end of use in HEP will be un-doubtfully achieved in the three years R&D program. A solid experience will be established in INFN on this innovative technology. Substantial progresses for the realization of a pixel chip for the HL_LHC are also guaranteed.

It could be found out, in the worst case, that the radiation hardness of the technology will not be sufficient for guaranteeing the survival of inner pixel layers for the whole period of HL_LHC (equivalent to the 3000 fb^{-1} of integrated luminosity) but this is not putting under discussion the HL_LHC pixel project: possibly a replacement of the affected layers can be foreseen before their performance becomes substantially deteriorated.

The risk that can be calculated is to fail the final goal of realizing a first prototype of sufficient scale, i.e. about 1x1 cm^2. This failure could be due to several reasons:

a) general delay in the schedule of the project
b) missing the finance for submitting the engineering run
c) the need for further R&D

Point b) could be due to missing a partner with which to share the submission of a engineering run. The estimated 300 ke allocated for the third year of the project, are sufficient for paying a 50% of a submission done using Multi-layer Mask service (MLM) provided by TSMC. Various project at CERN using 65nm, like the LP-GBT will be at a mature state for being interested in making the sharing of the submission, but it is too early for planning or discussing this.

A back-up plan, in case of not being able to proceed with a prototype, will be to continue with two MPW submissions one of which consists of a pixel chip array with reduced dimensions with respect to the prototype, but implementing new features compared to the submission of year 2015. This plan will still serve the goal of

pushing the R&D substantially, delaying the first engineering run by about one year. From the finance point of view, this implies a saving of about 100 keuro on the total cost of the project.

2.10 IMPACT ON RESEARCH AND HORIZON 2020

There are different topics that are closely related to the research work of CHIPIX65 and that can find their location in other fields other than an application for HEP experiment.

Radiation imaging pixel detector systems are also vital instruments in a large number of other research and development domains (medical Imaging, synchrotron light, material science, space science, radiation monitoring, x-ray fluorescence spectroscopy and astronomy) often using commercially available pixel detector systems. Such commercial pixel systems are to a large extent spin-offs from the development of novel pixel detectors in research institutes and universities. New pixel detector technologies are developed within CHIPIX. The dissemination of the developed pixel detectors and related technologies is an integral part of the proposal.

Hybrid pixel detectors consist of a separate pixelated sensor bump bonded to a high-density readout integrated circuit. The separation of the sensor and readout circuit enables sensors of different materials to be used (2D Si, 3D Si, CdTe, GaAs, Diamond, etc.) optimized for each specific application (e.g. x-ray or particles). In particular for very high rate applications the pixel sensor and the pixel readout integrated circuit can be optimized independently to obtain very high radiation tolerance and maintain 100% detection efficiency over the whole detector area (100% fill-factor). For comparison it can be mentioned that standard digital cameras have fill factors of ~50% and can only cope with very low frames rates (50Hz compared to 40MHz for LHC) and have no tolerance to radiation.

Radiation imaging devices and readout systems must function reliably over extended time periods in very harsh radiation environments. Total Ionising Dose (TID) of up to 10MGy generates large threshold shifts and leakage currents in the basic CMOS (Complementary Metal Oxide Semiconductor) transistors, unless an appropriate combination of technology choice and design approach is used. High neutron levels of up to 10^{16}neu/cm2 cause displacement damages in the silicon crystal lattice that in particular affects bipolar devices and optoelectronics devices (e.g. optical links). Finally, direct interactions between energetic particles and the atoms in the silicon of the electronics can induce enough charge locally to generate Single Event Upsets (SEU) corrupting the content of digital storage elements. Space applications are facing similar radiation effects. Commercial high reliability applications (e.g. automotive) are today also required to take into account SEUs, caused by natural background radiation, for critical functions implemented in deep sub-micron technologies.

As explain above, the research work made inside CHIPIX65 project can easily become part of a EU project, or stand for itself as autonomous proposal, to be submitted in the context of the Horizon2020 program. The collaborative network of CHIPIX65 among experts inside the project itself, or with international partners, like those of RD53, will easy substantially the process of building up a strong research group and a proposal on innovative electronics that can be submitted to Horizon2020. CMOS 65nm will still be of high interest even in a much larger community than HEP, for the next decade. The CHIPIX65 scientific project leader is committed to search for additional funding by submitting research proposals on topics related to this project, both in the context on national projects, like FIRB or PRIN, or European wide project funded by EU.

3 Additional Documentation

3.1 Letters of Endorsement

3.1.1 CMS

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
COMPACT MUON SOLENOID COLLABORATION
URL : http://cms.cern.ch

Adresse postale / Mailing address*:
Dr. Frank Hartmann
CMS Tracker Project Manager
CERN – PH Department
CH - 1211 GENEVA 23
Tel. *+41 76 487 4362*
Fax *+41 22 767 2277*
E-mail *Frank.Hartmann@cern.ch*
Dr. Didier Contardo
CMS Upgrade Coordinator
IN2P3 and CERN
IPN Lyon France
Tel. *+41 76 487 0608*
E-mail *Didier.Claude.Contardo@cern.ch*

INFN GR5

Italy

Geneva, July 14, 2013

Letter of support of the INFN R&D proposal CHIPIX65

The **CMS Collaboration** recognizes the challenges implied by the unprecedented conditions at which the CMS pixel detector should operate at the High Luminosity LHC.
In particular the pixel chip is a key element of the detector: its design and required performance is also related to the sensor choice, and to the global architecture of the front end, including the details of the readout chain and the possible contribution to the hardware DAQ triggering. The need of exploring larger scale integration CMOS technologies for the new pixel chip development is recognized, and the choice of 65nm CMOS, new in the HEP community, is strongly supported. The radiation hardness of the technology has to be quantified and is a common requirement for ATLAS and CMS; also several technical specifications are very similar between the two detectors.

Most of the INFN groups contributing to the CHIPIX65 proposal are also member of the international collaboration RD53 that has been approved recently by the LHCC committee and is also supported by the CMS Tracker. The purpose of the RD53 is to develop a pixel readout integrated circuit for extreme rate and radiation. We recognize that RD53 does not provide funding support for the R&D activities, each institute/country should contribute with funds provided by the its national agency. CHIPIX65 project, if approved, will be financed by INFN for four to six MPW submissions to the foundry.

We strongly support the formation of the INFN project CHIPIX65 and we actively endorse the collaboration with the **CMS Tracker Collaboration**

In short we unreservedly support the proposal

Sincerely Yours,

Frank Hartmann – CMS Tracker Project Manager

Didier Contardo – CMS Upgrade Coordinator

*Adresse postale pour le courrier posté en France : CERN : Site de Prévessin, F-01631 Prévessin Cedex

3.1.2 ATLAS

Dr. Natale Demaria
Coordinator of INFN Group V Call "CHIPIX65"
Istituto Nazionale di Fisica Nucleare - Sezione di Torino
Via Pietro Giuria, 1
I - 10125 Torino Italy
Email: lino.demaria@cern.ch

Professor Phil Allport
Director the Liverpool Semiconductor Detector Centre
Upgrade Coordinator on the ATLAS Experiment at the LHC
Department of Physics, University of Liverpool
Liverpool, UK
Email: allport@cern.ch

17th July 2013

Dear Natale,

For the CHIPIX65 project, we understand the related international proposal "Development of pixel readout integrated circuits for extreme rate and radiation" has led to the recent creation of an RD Collaboration. ATLAS strongly supports the proposed work, given the importance of shared efforts to keep costs down and because the relevant design expertise is a very scarce resource across our community. We also note that most of the digital design can be considered non-experiment specific and that this is by far the largest aspect. We recognise the need to focus on the development of basic building blocks, leaving open the specific optimizations finally required by each experiment. We note the relevance of this programme to possible MAPS/HV-CMOS developments in 65nm. The proposal focuses on the context of the extremely demanding environment for the pixel electronics in terms of rates and radiation levels anticipated at the HL-LHC. These challenges are major and the prototyping costs in 65nm are certainly high, making this proposed joint effort both timely and very well motivated.

The CHIPIX65 proposal addresses topics which are of great relevance to the longer term pixel detector developments of ATLAS and include areas with significant Italian leadership and industrial involvement.

Yours sincerely,

P P Allport

Prof Phil Allport
Upgrade Coordinator, ATLAS Collaboration

3.1.3 RD53

RD53 is an international collaboration with the purpose of developing pixel readout integrated circuits for extreme rate and radiation. The RD53 collaboration has been endorsed by the last LHCC committee and is composed of 17 institutes and 99 collaborators.

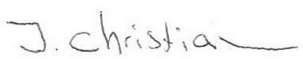
CHIPIX65 is a INFN three year project, subject to an approval by INFN in October 2013, with the goal of developing an innovative CHIP for a PIXel detector, using a 65nm CMOS technology, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. CHIPIX65 is composed of seven INFN units: Bari, Milano, Padova, Pavia, Perugia, Pisa, Torino. Six of this units have a strong link with CMS and one (Milano) with Atlas. It is composed of 33 members of whom 23 are IC designers. Six out of the seven research units of CHIPIX65 are already members of RD53. Milano has joined CHIPIX65 very recently and there has not yet been an opportunity to establish a formal involvement of Milano in RD53. We understand that CHIPIX65, if approved, is representing the INFN contribution to RD53.

RD53 does not provide financial support for the defined R&D activities. It will be based on contributions from each institute/country, provided by the national funding agencies. We understand that the CHIPIX65 project, if approved, will enable INFN to finance from four to six MPW submissions to the chosen foundry.

RD53 provides the collaboration framework to enable synergies at international level, sharing experience with worldwide HEP experts in the field and focused on this common interest. The RD53 collaboration will discuss and determine the best sub-division of work among participating members to guarantee the success of the defined R&D project. CHIPIX65 will be an integral part of this discussion and participation, representing the INFN expertise and contributions.

We believe that CHIPIX65 will make the contribution of the INFN groups stronger and self-consistent inside such an international R&D activity. This assures to maximize the overall results and experience obtained by the Italian groups in the context of using modern radiation tolerant CMOS technologies for front end electronics and in particular for future generation pixel chips required for the HL-LHC.

As RD53 convenors we strongly support the formation of the INFN project CHIPIX65 and we encourage the proposed collaboration with RD53. Further consolidation of the support will happen after the RD53 institution board have formalized and put in place its collaboration and management structure for the research and development program described in the R&D proposal to the LHCC: https://cds.cern.ch/record/1553467/



Jorgen Christiansen
CERN/ PH-ESE, Geneva, Switzerland

Maurice Garcia Sciveres
LBNL, Berkley California, USA

3.2 Letters of INFN Directors

3.2.1 Bari

INFN
ISTITUTO NAZIONALE DI FISICA NUCLEARE
Sezione di Bari
Il Direttore

Al Presidente della Commissione Scientifica Nazionale V dell'INFN
Prof. Massimo Carpinelli

Oggetto: Progetto CHIPIX65

Caro Massimo,

in relazione al progetto presentato in risposta alla "call" tematica della V Commissione con l'acronimo CHIPIX65 (Responsabile per la Sezione di Bari: ing. Flavio Loddo), che è stato discusso nel corso della riunione del Consiglio di Sezione del 5 luglio dedicata ai preventivi 2014, desidero comunicarti il mio parere positivo sull'iniziativa, e in particolare assicurarti che nulla osta per quanto riguarda l'utilizzo delle strutture e servizi della mia Sezione per lo svolgimento del progetto.

Resto a diposizione per ogni eventuale chiarimento.

Cordiali saluti,

Il Direttore
(*Prof. Mauro de Palma*)

INFN – Sez. di Bari - VIA G. AMENDOLA, 173 – 70126 BARI Telefoni: 080/5443200 – 5443201 – 5443202 – Fax +39 080 5534938

3.2.2 Milano

The director of Milano has expressed the support of the Sezione di Milano to CHIPIX65 project in the module EC/EN7 inside the Preventivi Data Base.

3.2.3 Padova

Istituto Nazionale
di Fisica Nucleare
Sezione di Padova

Il Direttore

Padova, 15 luglio 2013

Prof. Dario Bisello
Sede

Oggetto: Call CSN5 "CHIPIX65"

Caro Bisello,
con riferimento alla Call CSN5 "CHIPIX65" Le comunico che nullaosta all'eventuale utilizzo di risorse e/o di strumentazione della Struttura.

Cordiali saluti.

Dott. Mauro Mezzetto
Direttore

INFN - Sezione di Padova - Via F. Marzolo, 8 - 35131 PADOVA
Cod. Fisc. 84001850589 - Tel. +39 0499677127 – 7126 – 7160 – Fax +39 0498277111 – Info: http://www.pd.infn.it

3.2.4 Pavia

INFN
Istituto Nazionale di Fisica Nucleare
Sezione di Pavia

Pavia, 16 LUG. 2013
Via A. Bassi, 6 – 27100 Pavia – Italia

Prot. Nr. № - 0598

Pavia, 16 luglio 2013

Al. Prof. Massimo Carpinelli
Presidente Commissione V dell'INFN

OGGETTO: bando delle call di gruppo V – CHIPIX65

Facendo riferimento al progetto CHIPIX65 "Pixel Chip in 65nm CMOS Technology", esprimo parere positivo per l'eventuale utilizzo di risorse e/o strumentazione della Struttura INFN di Pavia.

Il Direttore
(Dr. Valerio Vercesi)

3.2.5 Perugia

Sezione di Perugia
INFN
Istituto Nazionale di Fisica Nucleare

Perugia, July 15, 2013

Al Prof. M. Carpinelli

Presidente della Commissione Scientifica Nazionale V

Caro Massimo,

In riferimento alla proposta progettuale di tipo "call" della CSN5 CHIPIX65 esprimo parere positive per l'eventuale utilizzo di risorse e/o di strumentazione della Struttura.

Cari saluti

Pasquale Lubrano

I.N.F.N. – Via A., Pascoli c/o Dip. Fisica Perugia – Tel. 075 5847137 – 075 5848237 – Fax 075 5847296

3.2.6 Pisa

INFN Istituto Nazionale di Fisica Nucleare

SEZIONE DI PISA

Istituto Nazionale di Fisica Nucleare
AOO: Sezione di Pisa
Partenza
Prot.N. 0000823 - 16/07/2013 - Tit. 3.5
Dest. Princ:
Dest. CC: Prof. Carpinelli CSN 5

Al Prof. Massimo Carpinelli
Presidente della Commissione Scientifica Nazionale V
INFN

Oggetto: Lettera di supporto per il bando delle call di Gruppo 5: CHIPIX65.

Caro Massimo,

facendo riferimento al progetto sigla CHIPIX65 'Pixel Chip in 65 nm CMOS technology' esprimo parere positivo per l'eventuale utilizzo di risorse e/o strumentazione della Struttura INFN di Pisa.

L'esperimento è di forte interesse e ben compatibile con le attività della sezione. In particolare sul personale la sezione potrà contribuire con un forte supporto (90% fte) di progettazione elettronica e 30% fte di tecnico del servizio Alte Tecnologie.

Cordiali saluti

Il Direttore della Sezione di Pisa

Prof. Giovanni Batignani

INFN – Largo Bruno Pontecorvo 3 - Pisa - Italy - Tel. 050 2214 000- Fax 050 2214 317 - Codice Fiscale n. 84001850589

3.2.7 Torino

INFN
Istituto Nazionale
di Fisica Nucleare
Sezione di Torino

Torino, 15 Luglio 2013

Al Prof. Massimo Carpinelli
Presidente Commissione V
INFN

OGGETTO - bando delle call di gr5 CHIPIX65.

Facendo riferimento al progetto sigla CHIPIX65 'Pixel Chip in 65nm CMOS technology' esprimo parere positivo per l'eventuale utilizzo di risorse e/o strumentazione della Struttura INFN di Torino.

IL DIRETTORE
(Dr. Amedeo Staiano)

via Giuria, 1 - 10125 TORINO – ITALY Tel. +39 011 655065 Fax. +39 011 6699579